A 1 GHz FLASH-ADC MODULE IN VMEbus

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Abstract

A data acquisition module based on monolithic high speed Flash-ADC chips (8 bit resolution) is described. Four fully independent channels, with 250 MHz sampling rate and a 2 KByte buffer memory each, can be combined (interleaved) in one channel to achieve an effective 1 GHz sampling rate with a total of 8 KByte memory depth. The double Eurocard board supports standard 16 bit or 32 bit VMEbus protocol for high speed readout. The board is essentially self contained and can be used cost effectively in small applications as in large experimental setups.

I. INTRODUCTION

Waveform sampling or transient recording has proven to be a major advancement in analyzing and processing of detector signals in physics research. Large experiments with their need for setups which are optimized in price and performance have led in our institute to specifically designed data acquisition systems (e.g. DL300) [1]. Such systems found already a large application in high energy physics experiments (JADE,OPAL) for improved time and double pulse resolution [1),2),3)]. Smaller experimental applications on the other hand rely on standard bus systems like the popular VMEbus and have already led to a modular data acquisition system based on fast 100 MHz flash-Analog-to-Digital-Converters (FADCs) [4].

Now the availability of even faster FADC chips made a new design possible (DL515) to achieve sampling rates of up to 1 GHz on a standard VME board. This performance is comparable to the fastest digital transient recorders on the market at a much lower price and is well suited for time critical wave form or pulse shape analysis in the laboratory.

A first physics application in our institute needs the high time resolution for recording and evaluating "chirp" signals which occur during the amplification of a highly frequency stable cw dye laser in a pulsed dy laser amplifier. A heterodyne beat signal from a photodiode of typically 250 MHz has to be recorded within the 15 ns long laser pulse.

II. SPECIFICATIONS

The following Table 1 gives an overview about the main parameters of the DL515 digitizer board.

Parameter	Value
Number of channels on board	4
Sampling rate / channel	≤ 250 MHz
max. Sampling rate (interleaved)	1 GHz
Amplitude resolution	8 bit
Analog bandwidth	400 MHz
Input range	0V…-2V
Input impedance	10 kΩ
Memory depth (total)	8 KBytes
Readout speed / longword (VMEbus)	100ns

Table 1: DL515 Specifications.

III. FADC CIRCUITRY

Figure 1 shows the layout of the different function blocks on the VME board (double Eurocard, single width), the analog channel inputs and control connectors (NIM) at the frontpanel and the bus and power connectors on the rear.

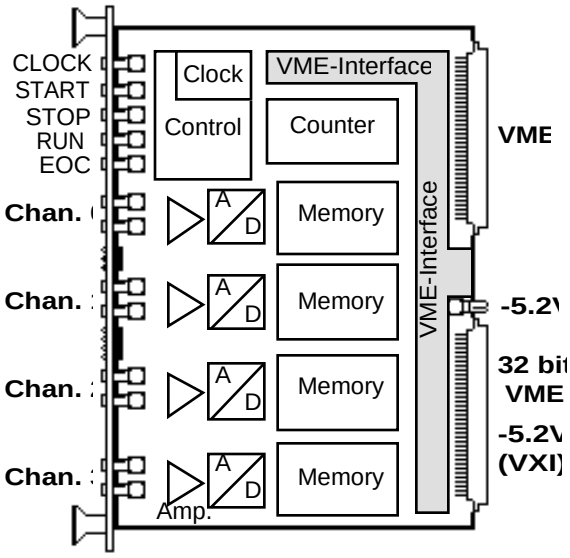

Fig. 1: Layout of DL515 Flash-ADC board.

The VME board houses 4 complete FADC channels with the following subcircuits:

A. Control

The module is mainly controlled by two external input signals (START, STOP) and provides two status output signals (RUN, EndOfConversion) as seen in figure 2. All these signals are located at the frontpanel, additionally they can be set or accessed by software. For different applications the module supports selectable modes to realize AutoReset after start, AutoStop after memory overrun and the generation of interrupts after conversion.

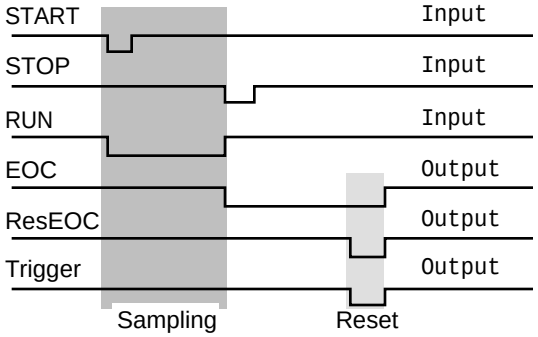

Fig.2.: DL515 Control signals.

B. Clock

All four FADC channels digitize the inputs in parallel and are driven by a common system clock of up to 300 MHz. Right now an onboard quartz stabilized oscillator with 250 MHz is used. The clock could also be replaced by a start/stop delay clock or can be supplied from an external source.

C. FADC channel

Each channel consists of an analog buffer amplifier, the FADC chip with 8 bit amplitude resolution and a two fold memory bank of 1 KByte to store the data. The FADC chip (AD9038 from Analog Devices) contains already two output latches to demultiplex the data rate by half (to 125 MHz) for the ECL memories.

D. Address Counter

A 10 bit counter generates all the address signals for the memories. As it can be read out after conversion it can also be used as a time reference in CommonStop mode. In Non AutoReset mode the address counter will be retained after stop and recording will simply continue after a new start realizing multi event buffering.

E. VME interface

All fast electronics on the board is in ECL technology and needs level conversion to TTL for address, data and control signals to and from VME. The following memory map in table 2 shows how the module can be programmed and read out ($E00000 is base address!). The access to the memories and control registers is arbitrary and supports both 16 bit and 32 bit VME transfers for fast readout of the stored digitized data.

	Highword	Lowword	
WRITE:	D31 ……	D15 …… D0	
$E08000			Software **Start**
$E08004			Software **Stop**
$E08008			**ResEOC** / Trigger
$E0800C	D0	D0	set **Autostop**

READ:					
$E00000	Ch3	Ch2	Ch1	Ch0	**Data** Sample 0
$E00004	Ch3	Ch2	Ch1	Ch0	**Data** Sample 1
…	…	…	…	…	…
$E01FFC	Ch3	Ch2	Ch1	Ch0	**Data** Sample 2047

$E08000	D9…D0=AC D14= EOC D15= RUN	D9…D0=AC D14= EOC D15= RUN	**Address Counter** & **Status**

Table 2: DL515 Memory Map.

IV. 1 GHz Operation

To achieve an effective sampling rate of 1 GHz the four channels operated at 250 MHz each have to be interleaved in time. This is done very easily by feeding all four channels in parallel to the analog inputs and delaying the signal from one channel to the next for 1 ns.

One possibility would be to split the input signal into four separate channels which have to be delayed accordingly with 0 ns, 1 ns, 2 ns and 3 ns. A passive splitter however decreases the analog amplitude at each channel by half.

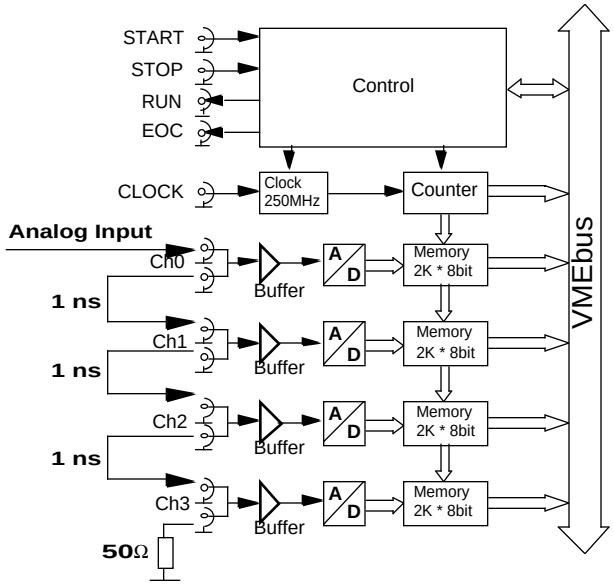

Fig. 3: DL515 Blockdiagram, combining 4 channels into 1 channel interleaved mode.

Another possible configuration can be seen in the blockdiagram in figure 3. The analog signal is bypassed at high impedance inputs, delayed and terminated at the end. The advantage of this setup is no amplitude loss and the use of only equal delay cables.

Figure 4 with a heavily distorted impulse from a (intentionally) not terminated transmission line shows how the data in the time interleaved four channels contribute to one complete picture of the impulse.

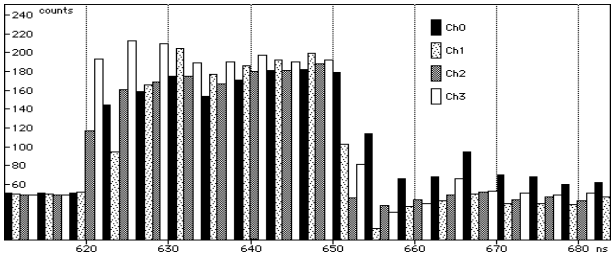

Fig. 4: Channel correspondence in interleaved mode.

The interleaving of four individual 250 MHz channels into one channel in order to get an effective sampling rate of 1 GHz makes only sense if the analog bandwidth of each channel is high enough. The following plot in figure 5 with the large signal (full range) frequency response of the FADC channels shows a cutoff frequency around 400 Mhz. This indicates sufficient bandwidth (nearly up to the Nyquist edge) to transmit high frequency information.

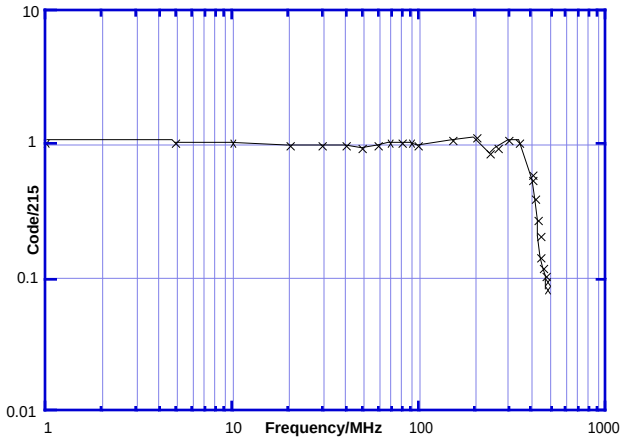

Fig. 5: Large signal Frequency Response

V. PERFORMANCE

The DL515 FADC module exists now already in several samples and its performance has been tested in different aspects. Especially the performance of running the module as a 1 GHz ADC and the needed time resolution is important for the present foreseen application and will be discussed further on.

A. FFT Tests

A very common test of the performance of fast ADCs is the fourier spectrum analysis. As an example a 50 MHz sine wave was digitized in the interleaved mode, weighted with a Hanning window and transformed into the frequency domain via FFT (figure 6).

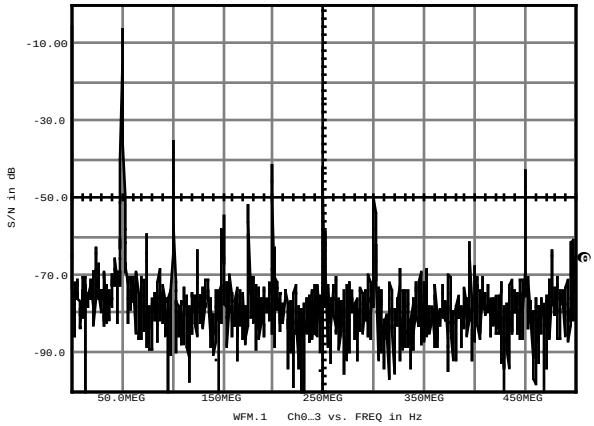

Fig. 6: FFT of 50 MHz sine at 1 GHz sampling rate.

It is not easy to evaluate correct numbers from the FFT with energy spreading and folding back or aliasing of harmonics. This is due to the discrete transformation (DFT) with a finite record size [5]. In general the FFT shows the influences of converter errors in two important parameters:

SNR (signal to noise ratio): Noise is mainly induced by the time and amplitude discrete digitization (the quantization error) but also through other errors like e.g. differential non-linearities and aperture jitter or errors in the analog chain. The SNR can be used to calculate the number n of effective bits of the conversion (SNR = n/bits * 6.02 dB + 1.8dB).

THD (total harmonic distortion): Mainly integral non-linearities lead to an increase of harmonic components in the spectrum. The relatively high harmonics (≤ 35dB) in the spectrum could be caused by a mismatch in the amplitudes of the four channels which could be corrected by software.

B. Histogram Tests

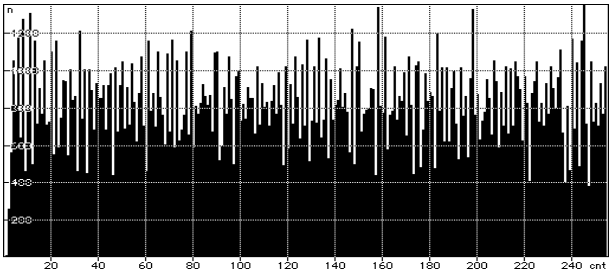

Fig. 7: Code histogram of a ramp input signal.

A simple code histogram of a ramp signal covering the whole amplitude range exhibits more clearly some linearity properties of the digitization (figure 7). No missing codes are observed here. The relatively high value for the differential nonlinearity (< 0.5 LSB) is a typical value for flash converters and impairs applications with demand for equal code distribution and monotonicity (e.g. amplitude spectroscopy).

C. Time resolution

The following example of a digitized single pulse with significant pulse ringing shows very clearly the improvement with the four times greater time resolution in the 1 GHz interleaved mode (figure 9) compared to the basic 250 Mhz sampling data provided by only one channel (figure 8).

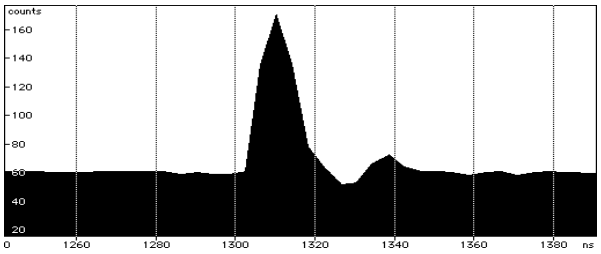

Fig. 8: FADC raw data with 250 MHz sampling rate.

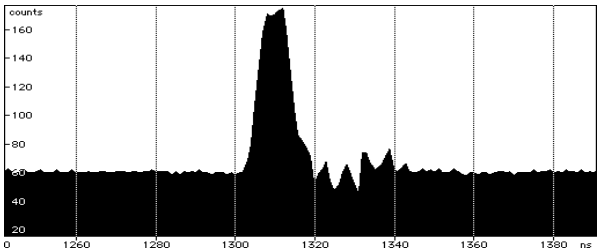

Fig. 9: FADC raw data with 1 GHz sampling rate.

Another example in figure 10 shows a recorded 1 MHz square wave. A close-up of the data in figure 11 at the falling edge of the signal reveals some subtle details. In figure 12 a very narrow pulse was applied to the FADC module and sampled in interleaved mode. To improve the resolution, especially to increase the signal to noise ratio, the data of several (20) digitization shots were averaged in one picture.

VI. CONCLUSION

By using standard electronic components it was possible to build a high performance but compact digitizer module. The given examples show the usefulness of the converter module operated in interleaved mode to get a very high sampling rate which compares to the fastest digital oscilloscopes on the market (LeCroy, DSP, Analytek, HP, Tek, ...).

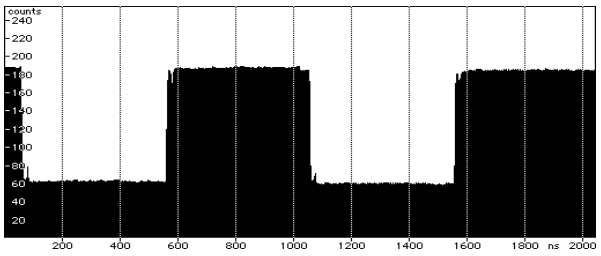

Fig. 10: FADC raw data of square wave.

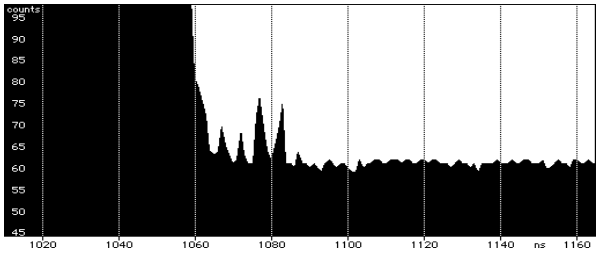

Fig. 11: Close-up of pulse ringing after falling edge.

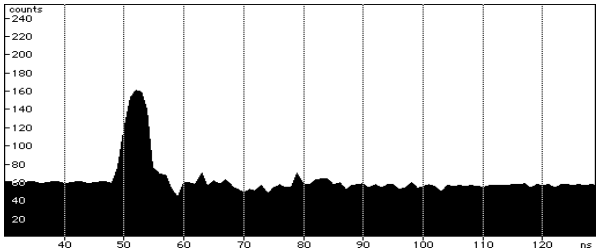

Fig. 12: 5 ns pulse at 1 GHz recorded and over 20 samples averaged.

VII. REFERENCES

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